Winstar Display Co., LTD
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SPECIFICATION

MODULE NO.: WF57ETIACDNN0#

General Specifications

Item	Dimension	Unit
Size	5.7	inch
Dot Matrix	320 x RGBx240(TFT)	dots
Module dimension	141.12(W) x 101.55(H) x 6.5(D)MAX	mm
Active area	115.2 x 86.40	mm
Dot pitch	0.12 x 0.36	mm
LCD type	TFT, Normally White, Transmissive	
View Direction	12 o'clock	
Gray Scale Inversion Direction	6 o'clock	
Backlight Type	LED, Normally White	
With /Without TP	Without TP	
Surface	Glare	

*Color tone slight changed by temperature and driving voltage.

Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-20	—	+70	℃
Storage Temperature	TST	-30	—	+80	℃

Electrical Characteristics

Operating conditions:

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VCC	—	3.0	3.3	3.6	V
Input High Volt.	V_{IH}	—	0.7 Vcc	—	Vcc	V
Input Low Volt.	V_{IL}	—	0	—	0.3 Vcc	V
LCD Driving Supply Voltage	V_{GH}*1	Ta=25℃		15		V*3
	V_{GL}*2			-10		
	VcomH		2.5		5.5	
	VcomL		-2.0		0	
Supply Current	I_{VCC}	VCC=3.3V	—	5	8	mA

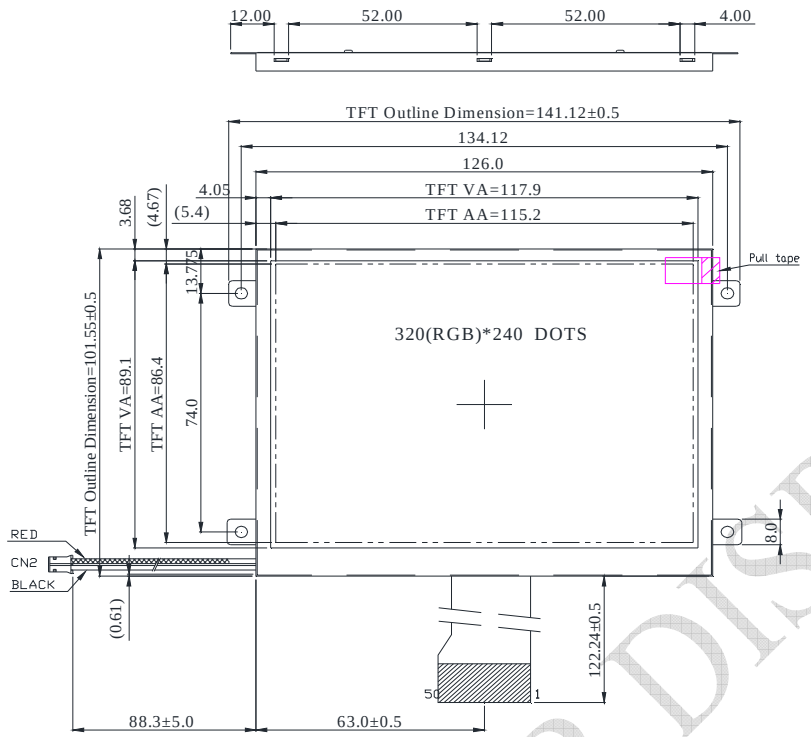
Interface

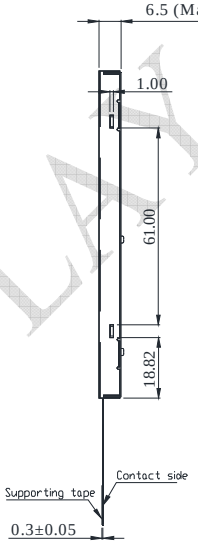
LCM PIN Definition

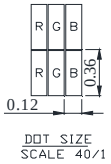
Pin	Symbol	Function
1	IF1	Input data format control
2	IF2	Input data format control
3	POL	Polarity Signal connect to VCOM driving circuit.
4	RESET	Hardware reset
5	SPENA	Chip select
6	SPCL	Serial Clock
7	SPDA	Serial Data
8	B0	Blue Data bit
9	B1	Blue Data bit
10	B2	Blue Data bit
11	B3	Blue Data bit
12	B4	Blue Data bit
13	B5	Blue Data bit
14	B6	Blue Data bit
15	B7	Blue Data bit
16	G0	Green Data bit
17	G1	Green Data bit
18	G2	Green Data bit
19	G3	Green Data bit
20	G4	Green Data bit
21	G5	Green Data bit
22	G6	Green Data bit
23	G7	Green Data bit
24	R0	Red Data bit
25	R1	Red Data bit
26	R2	Red Data bit
27	R3	Red Data bit
28	R4	Red Data bit
29	R5	Red Data bit
30	R6	Red Data bit
31	R7	Red Data bit
32	Hsync	Horizontal synchronous signal
33	Vsync	Vertical synchronous signal
34	Data CLK	Dot data clock
35	AVDD(analog)	Analog power: 4.5V~5.5V
36	AVDD(analog)	Analog power: 4.5V~5.5V

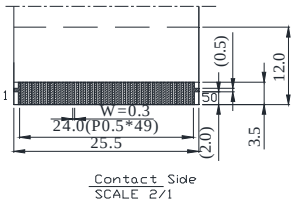
37	VCC(Digital)	Digital power: 3V~3.6V
38	VCC(Digital)	Digital power: 3V~3.6V
39	NPC	NTSC/PAL mode Auto detection result H:NTSC/L:PAL
40	VGL	Gate off power
41	VGL	Gate off power
42	UD	Up/down selection
43	VGH	Gate on power
44	LRC	Shift direction of device internal shift register control.
45	GND	System ground pin of the IC. Connect to system ground.
46	VCOM	VCOM driving input
47	VCOM	VCOM driving input
48	ENB	Signal to settle the horizontal display position
49	GND	System ground pin of the IC. Connect to system ground.
50	GND	System ground pin of the IC. Connect to system ground.

Contour Drawing









PIN NO	SYMBOL	PIN NO	SYMBOL	PIN NO	SYMBOL
1	IF1	21	G5	41	VGL
2	IF2	22	G6	42	UD
3	POL	23	G7	43	VGH
4	RESET	24	R0	44	LRC
5	SPENA	25	R1	45	GND
6	SPCL	26	R2	46	VCOM
7	SPDA	27	R3	47	VCOM
8	B0	28	R4	48	ENB
9	B1	29	R5	49	GND
10	B2	30	R6	50	GND
11	B3	31	R7		
12	B4	32	Hsync	CN2	
13	B5	33	Vsync	RED	+
14	B6	34	Data CLK	BLACK	−
15	B7	35	AVDD(analog)		
16	G0	36	AVDD(analog)		
17	G1	37	Vcc(Digital)		
18	G2	38	Vcc(Digital)		
19	G3	39	NPC		
20	G4	40	VGL		

The non-specified tolerance of dimension is ±0.3mm.