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GI FAR TECHNOLOGY CO.,LTD
No. 81, Dongfeng St, Shulin District, 23874, New Taipei City, Taiwan, R.O.C.

SPECIFICATIONS

CUSTOMER : _____

MODEL NO. : GFE122032H-GPFE

VERSION : D

DATE : 2017.03.24

CERTIFICATION : ROHS

CUSTOMER SIGN : _____

QA Approved By	Approved By	Prepared By	Prepared By
	GIFAR 2017.03.27 Donlin	GIFAR 2017.03.27 Jerry	GIFAR 2017.03.27 Hazel

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Revision Record

Data(y/m/d)	Ver.	Description	Note	page
2012.05.10	A	Specification released		
2012.07.03	B	圖面備註增加背光限流電阻 0R*2		**19**
2014.08.19	C	1. 修正背光規格 2. 19pin 處備註(+3.5V)		**6、9**
2017.03.24	D	修改公司抬頭、格式統一		

CONTENTS

1. SCOPE

This specification covers the engineering requirements for the GFE122032H-GPFE liquid crystal module.

2. PRODUCT SPECIFICATIONS

2.1 General

- 122 × 32 dot matrix LCD
- **STN (GRAY)**, **Positive** mode LCD panel
- **Transflective** Wide temperature type
- 6 o'clock
- Multiplexing driving : 1/32duty, 1/6bias
- Controller IC : **SBN1661G** or Compatible
- Backlight: **WHITE(EDGE)**

2.2 Mechanical Characteristics

Item	Value	Unit
Number of dots	122X32	Dot
Dot size	0.4 X0.45	mm
Dot pitch	0.44 X0.49	mm
Module dimension	80(W) X 36(H) X 13.7(T)	mm
Viewing Area	60 (W) X 18 (H)	mm
Active Area	53.64 (W) X 15.64 (H)	mm
Module	NO Connector	
Remark	Backlight 限流電阻 0R*2	

2.3 Absolute Maximum Ratings (Without LED back-light)

Characteristic	Symbol	Unit	Value
Operating Voltage (logic)	V_{DD}	V	-0.3 to +7.0
Input Voltage	V_{IN}	V	-0.3 to V_{DD}+0.3

Note 1: Referenced to V_{SS}=0V

2.4 Electrical Characteristics (Without LED back-light)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage(logic)	V_{DD}-V_{SS}	--	4.7	5.0	5.3	V
Input Voltage	V_{IH}	--	0.8V_{DD}	--	V_{DD}	V
	V_{IL}	--	V_{SS}	--	0.2V_{DD}	
Output Voltage	V_{OH}	I_{OH}=-0.1mA	0.8V_{DD}	--	V_{DD}	V
	V_{HL}	I_{OL}=0.1mA	V_{SS}	--	0.2V_{DD}	

2.5 Optical Characteristics Absolute maximum ratings

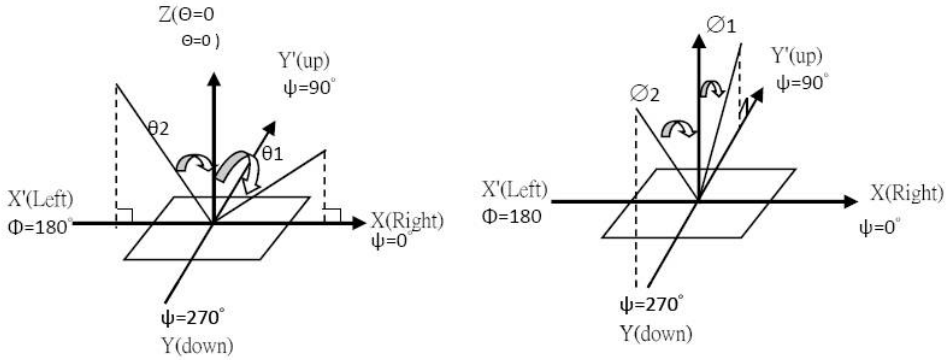
Item	Symbol	Rating	Unit
Operating temperature range	Top	-20~70	°C
Storage temperature range	Tst	-30~80	°C

2.6. Optical Characteristics

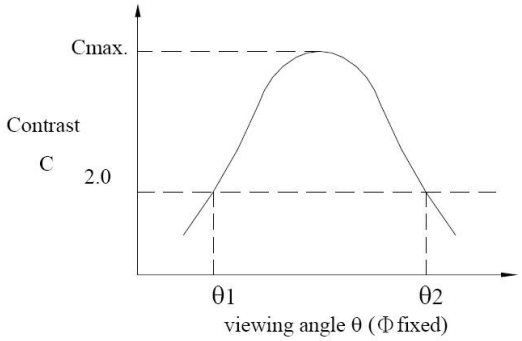
1/32 duty, 1/6 bias, Vop=4.6 V, Ta=25℃

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Driving voltage	Vop		--	4.6	--	
Viewing angle	θ1、θ2	C≥2.0,∅=0° C	30°	-	-	Notes 1 & 2
Contrast	C	θ=5°, ∅=0°	2.0	-	-	Note 3
Response time(rise)	ton	θ=5°, ∅=0°	-	176	260ms	Note 4
Response time(fall)	toff	θ=5°, ∅=0°	-	250	380ms	Note 4

Note 1: Definition of angles θ and ∅

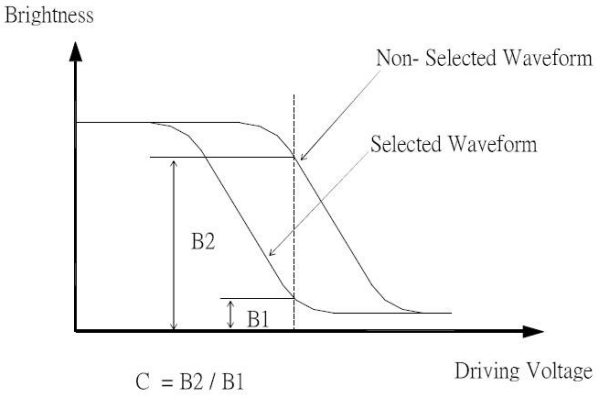


Note 2: Definition of viewing angles θ1 and θ2



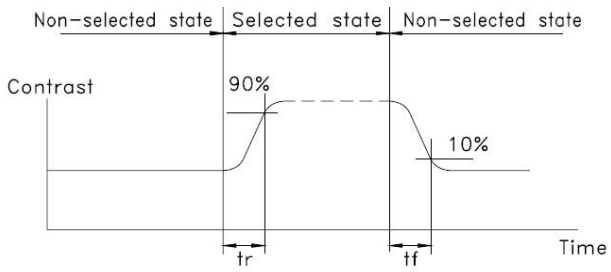
Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the same

Note 3: Definition of contrast C



C = B2 / B1

Note 4: Definition of response time



Note: Measured with a transmissive LCD panel which is displayed 1 cm^2

V_{OPR} : Operating voltage f_{FRM} : Frame frequency
t_{ON} : Response time (rise) t_{OFF} : Response time (fall)

2.7 LED Back-light Characteristics

2.7.1 Electrical / optical specifications

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	V_f	If=40mA, WHITE	2.9	3.1	3.3	V
*Luminous Intensity	I_V	If=40mA, WHITE	850	1000	--	cd/m^2
Peak wavelength	λP	If=40mA, WHITE	0.26 0.26	0.28 0.28	0.30 0.30	nm
Spectrum Radiation Bandwidth	Δλ	If=40mA, WHITE	--	30	--	nm
Reverse Current	I_R	VR=5V, WHITE	--	--	0.04	Ma
Illuminance power deviation	△ EH	If=40mA, WHITE	75			%
Luminous Uniformity	ΔLv	If=40mA, WHITE	70			%

Note: * Please refer to CIE 1931 Chromaticity diagram.

2.7.2 LED Maximum Operating Range

Item	Symbol	Yellow-Green	Unit
Power Dissipation	P_{AD}	165	mW
Forward Current	I_F	50	mA
Reverse Voltage	V_R	5	V

3. RELIABILITY

NO.	ITEM	CONDITION		STANDARD	NOTE
1	High Temp. Storage	80℃	120 hrs	Appearance Without defect	
2	Low Temp. Storage	-30℃	120 hrs	Appearance Without defect	
3	High Temp. & High Humi. Storage	40℃ 90% RH	120 hrs	Appearance Without defect	
4	High Temp. Operating Display	70℃	120 hrs	Appearance Without defect	
5	Low Temp. Operating Display	-20℃	120 hrs	Appearance Without defect	
6	Thermal Shock	-20℃, 30min. → 70℃,30min. (1cycle)		Appearance Without defect	10 cycles

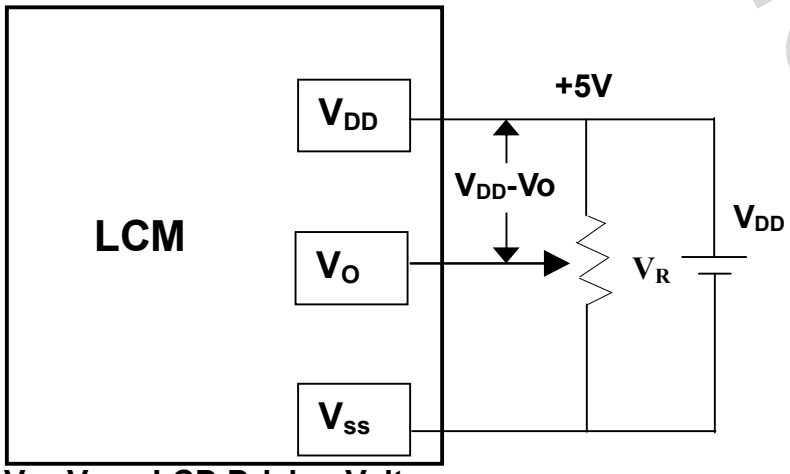
** Dissipation current, contrast and display functions
** Polarizing filter deterioration, other appearance defects
** The function test shall be conducted after 4hours storage at the normal temperature and humidity after remove from the test chamber.

4. OPERATING INSTRUCTIONS

4.1 Input signal Function

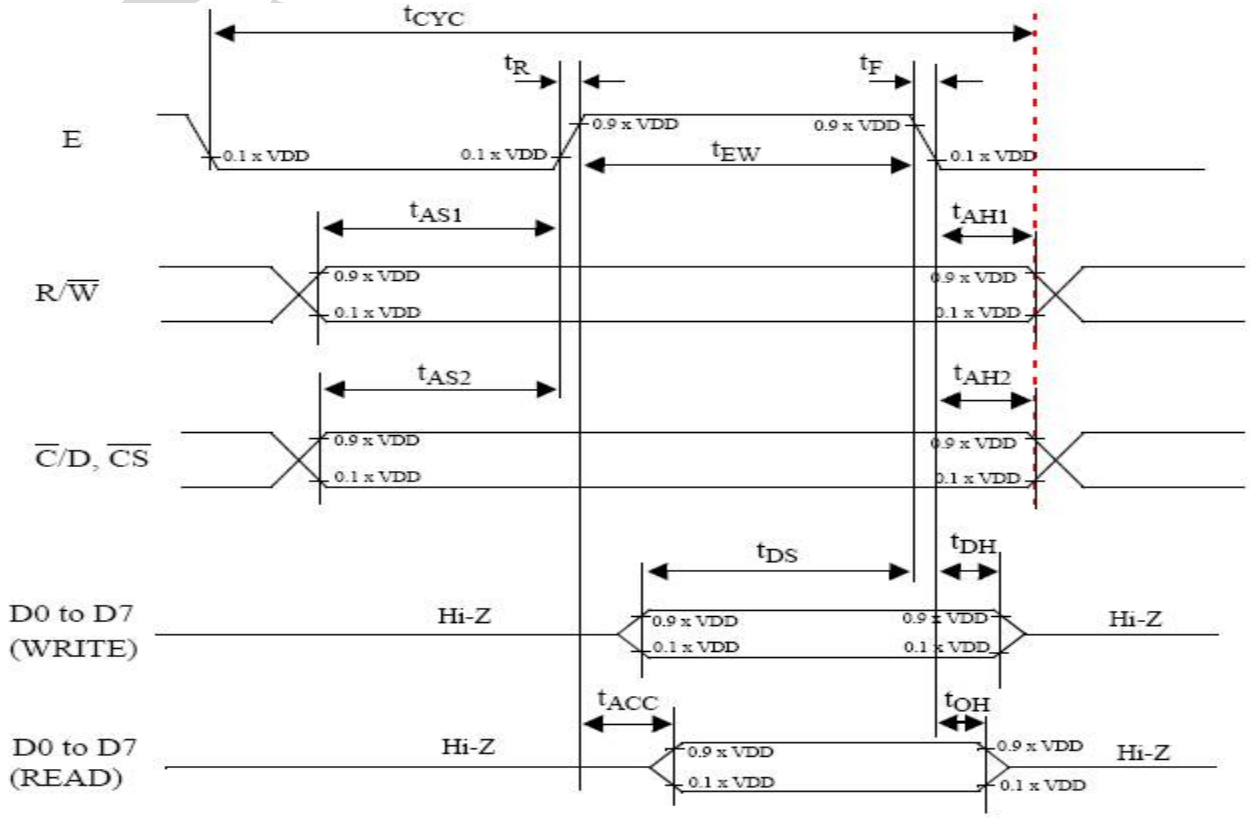
Pin No	Symbol	Function
1	Vss	Signal ground (GND)
2	Vdd	Power supply for logic (+5V)
3	Vo	Operating voltage for LCD (variable)
4	A0	Start enable signal to read or write the data
5	CS1	Chip1 enable (segment 1 to segment 64),Active high
6	CS2	Chip2 enable (segment 65 to segment 128),Active high
7	NC	NC
8	NC	NC
9	R/W	Data read & write
10-13	DB0~DB3	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCD module.
14-17	DB4~DB7	Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCD module. DB7 can be used as a busy flag.
18	RST	Reset signal
19	A/VEE	LED backlight drive voltage V+ (+3.5V)
20	K	LED backlight drive voltage ground

4.2 Voltage Generator Circuit



V_{DD}-Vo : LCD Driving Voltage
V_R : 10K~20K

4.3 Timing Diagram



symbol	parameter	min.	max.	test conditons	unit
t_{AS1}	Address set-up time with respect to R/$\overline{W}$	20			ns
t_{AS2}	Address set-up time with respect to $\overline{C}$/D, $\overline{CS}$	20			ns
t_{AH1}	Address hold time with respect to R/$\overline{W}$	10			ns
t_{AH2}	Address hold time respect with to $\overline{C}$/D, $\overline{CS}$	10			ns
t_F, t_R	Enable (E) pulse falling/rising time		15		ns
t_{CYC}	System cycle time	1000		Note 1	ns
t_{EWR}	Enable pulse width for READ	100			ns
t_{EWW}	Enable pulse width for WRITE	80			ns
t_{DS}	Data setup time	80			ns
t_{DH}	Data hold time	10			ns
t_{ACC}	Data access time		90	CL= 100 pF.	ns
t_{OH}	Data output hold time	10	60	Refer to Fig. 23.	ns

4.4.DISPLAY CONTROL INSTRUCTIONS AND REGISTERS

4.4.1 Registers and their states after hardware RESET

The SBN1661G_X has a set of registers. To ensure proper operation of the devices, these registers must be programmed with proper values after hardware reset.

The registers and their states after RESET is given in Table 1.

Table 1 Registers and their states after RESET

Register Name	Description	States after RESET
Display ON/OFF Register	The Display ON/OFF Register is a 1-bit register. After RESET, its value is LOW and, therefore, the LCD display is turned OFF.	0
Display Start Line Register	The Display Start Line Register is a 6-bit register. After RESET, its value is 0 0000 and Row0 of the Display Data Memory is mapped to COM0.	00 0000
Page Addres Register	The Page Address Register is a 3-bit register. After RESET, its value is 11 and, therefore, it points to Page 7 of the Display Data Memory.	111
Column Address Register	The Column Address Register is a 7-bit register. After RESET, its value is 000 0000 and, therefore, it points to column 0 of the Display Data Memory.	000 0000
Static Drive ON/OFF Register	The Static Drive ON/OFF Register is a 1-bit register. After RESET, its value is LOW and static display is turned OFF.	0
Duty Select Register	The Duty Select Register is a 1-bit register. After RESET, its value is HIGH and 1/32 display duty is selected.	1
Column/Segment Mapping Register	The Column/Segment Mapping Register is a 1-bit register. After RESET, its value is LOW and normal mapping is selected.	0
Status Register	The Status Register shows the current state of the SBN1661G_X. It is a 4-bit register, with each bit showing the status of a programmed function.	0000 0000

4.4.2 Display ON/OFF and the Display ON/OFF Register

The Display ON/OFF Register is a 1-bit Register. When this bit is progammed to HIGH, the display is turned ON. When this bit is programmed to LOW, the display is turned OFF and all COMMON and SEGMENT outputs are set to VDD.

To program this register, the setting of control bus is given in Table 2 and the setting of the data bus is given in Table 3.

Table 2 Setting of the control bus for programming the Display ON/OFF Register

C/D	E/(RD)	R/W(WR)
0	1	0

Table 3 Setting of the data bus for programming the Display ON/OFF Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	0	1	0	1	1	1	D0

When D0=1, the code is AF(Hex) and the display is turned ON. When D0=0, the code is AE(Hex) and the display is turned OFF.

4.4.3 Display Start Line and the Display Start Line Register

The Display Start Line Register is a 5-bit Register. It points at the first row of a block of the Display Data Memory, which will be mapped to COM0. The length of the block of the memory can be 32 rows or 16 rows, which is decided by the Duty Select Register. For example, if the Display Start Line Register is programmed with 00010 (decimal 2) and display duty is 1/32, then Row2 of the Display Data Memory will be mapped to COM0 of LCD panel, Row3 to COM1, Row4 to COM2, Row30 to COM28, Row31 to COM29, Row0 to COM30, and finally Row1 to COM31, as illustrated in Fig. 11. However, in this case, only Row2~Row17 can be displayed on COM0~COM15, as COM16~COM31 are not availabe from the chip.

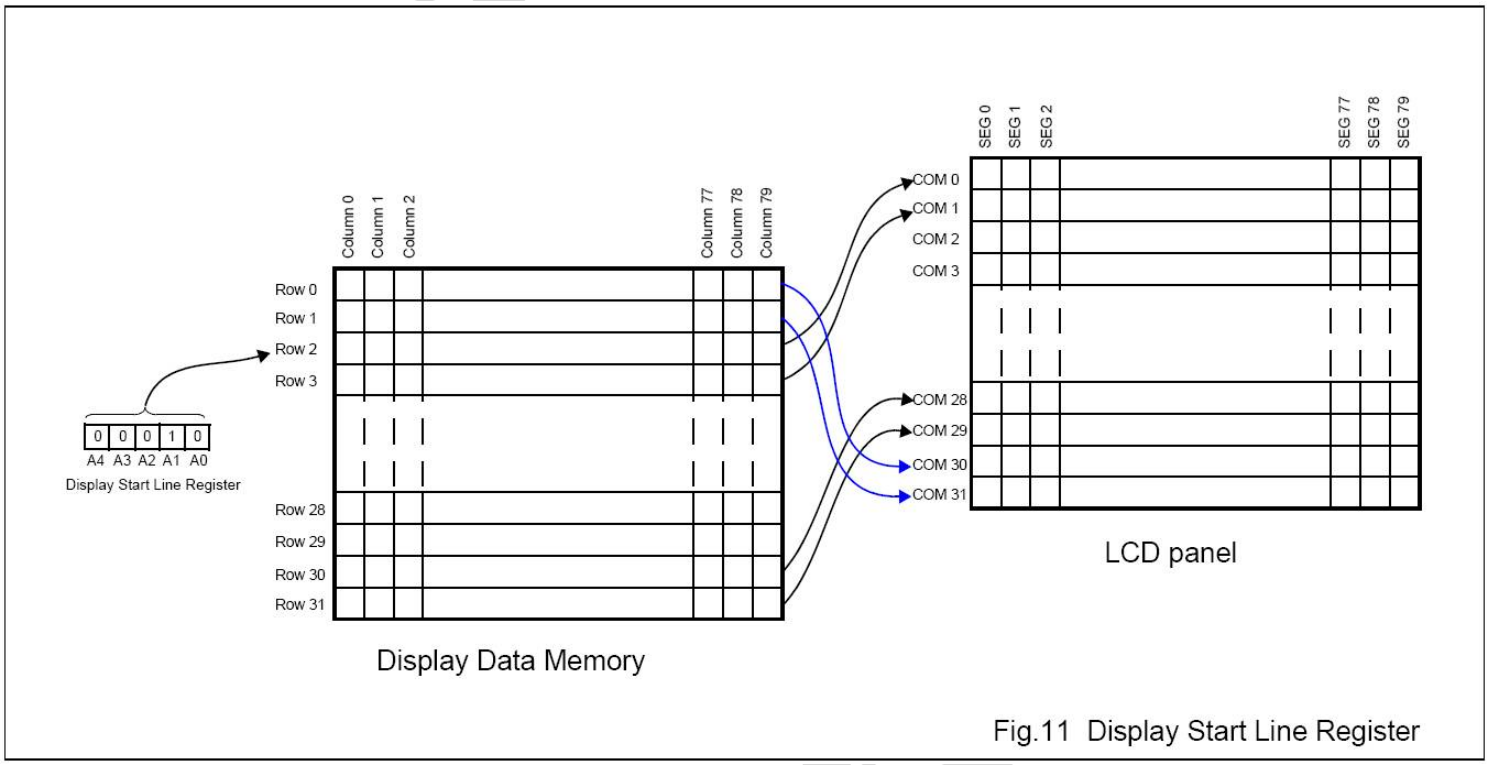


Fig.11 Display Start Line Register

To program this register, the setting of the control bus is given in Table 4 and the setting of the data bus is given in Table 5.

Table 4 The setting of the control bus for programming the Display Start Line Register

C/D	E/(RD)	R/W(WR)
0	1	0

Table 5 The setting of the data bus for programming the Display Start Line Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	1	0	A4	A3	A2	A1	A0

A4, A3, A2, A1, and A0 are Start Line address bits and they can be programmed with a value in the range from 0 to 31. Therefore, the code can be from 1100 0000 (C0 Hex) to 1101 1111 (DF Hex).

4.4.4 Display Data Memory Page and the Page Address Register

The on-chip Display Data Memory is divided into 4 pages: Page 0, Page 1, Page 2, and Page 3, with each page having 80 bytes in horizontal direction. Page 0 is from Row 0 to Row 7, Page 1 from Row 8 to Row 15, Page 2 from Row 16 to Row 23, and Page 3 from Row 24 to Row 31, as shown in Fig 12. When the host microtroller intends to perform a READ/WRITE operation to the Display Data Memory, it has to program the Page Adrress Register to indicate which page it intends to access.

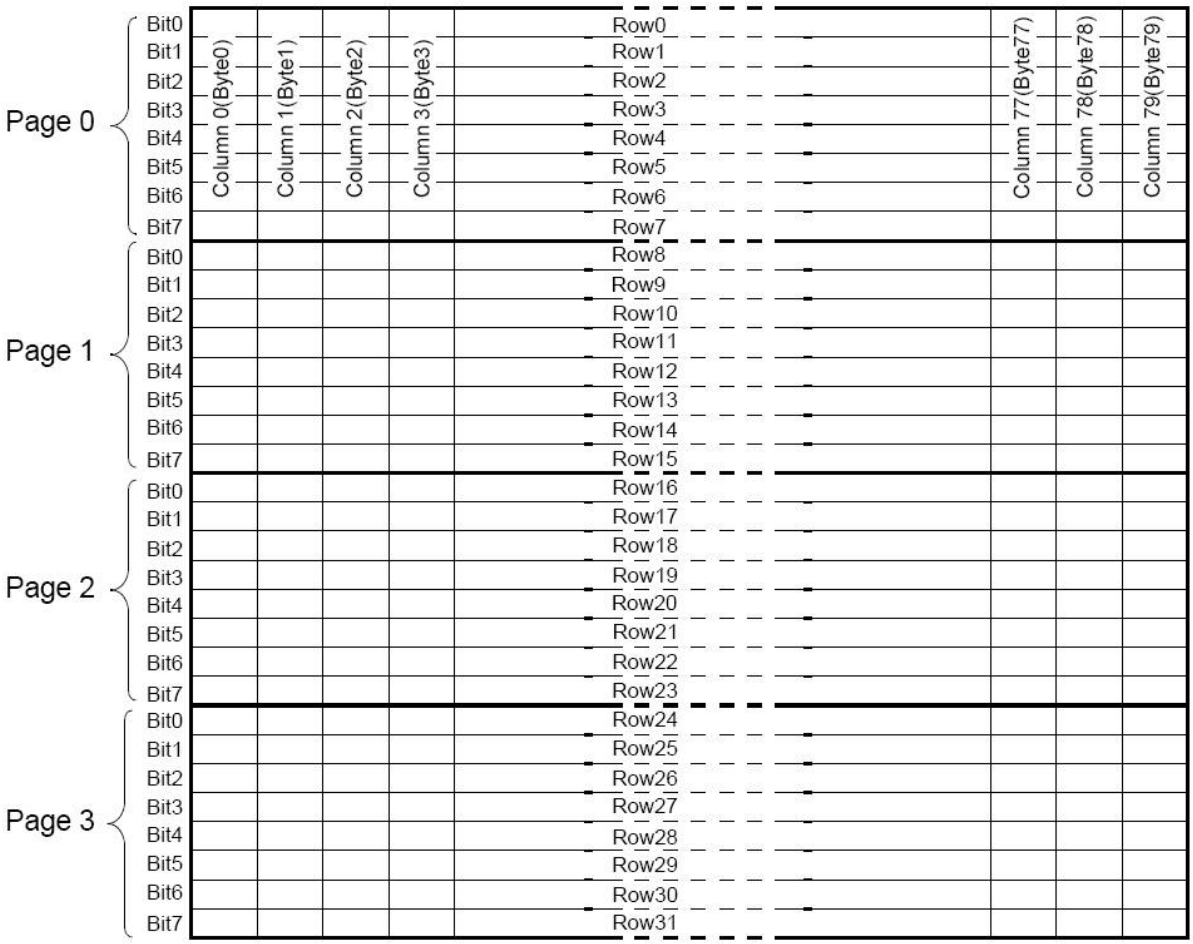


Fig.12 Page/Column allocation of the Display Data Memory

To program this register, the setting of the control bus is given in Table 6 and the setting of the data bus is given in Table 7.

Table 6 The setting of the control bus for programming the Page Address Register

C/D	E/(RD)	R/W(WR)
0	1	0

Table 7 The setting of the data bus for programming the Page Address Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	0	1	1	1	0	A1	A0

A1and A0 are page address bits and can be programmed with a value in the range from 0 to 3. A1A0=00 selects Page 0, A1A0=01 selects Page 1, A1A0=10 selects Page 2, and A1A0=11 selects Page 3. Therefore, the code can be from 1011 1000 (B8 Hex) to 1011 1011 (BB Hex).

4.4.5 Column address and the Column Address Register

The Column Address Register points at a column of the Display Data Memory which the host microcontroller intends to perform a READ/WRITE operation. The Column Address Register automatically increments by 1 after a READ or WRITE operation is finished. When the Column Address Register reaches 79, it overflows to 0. Please refer to Fig.12 for the column sequence in a page of the Display Data Memory.

To program this register, the setting of the control bus is given in Table 8 and the setting of the data bus is given in Table 9.

Table 8 The setting of the control bus for programming the Column Address Register

C/D	E/(RD)	R/W(WR)
0	1	0

Table 9 The setting of the data bus for programming the Column Address Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
0	A6	A5	A4	A3	A2	A1	A0

A6~A0 are column address bits and can be programmed with a value in the range from 0 to 79. Therefore, the code can be from 0000 0000 (00 Hex) to 0100 1111 (4F Hex).

4.4.6 Mapping between Memory Cloumns and Segments and the Column/Segment Mapping Register

The Column/Segment Mapping Register is a 1-bit register and selects the mapping relation between the column outputs of the Display Data Memory and the Segment outputs SEG0~SEG79.

If this register is programmed with HIGH, then the data from column 79 of the Display Data Memory will be output from SEG0. This type of mapping is called *inverted mapping*.

If this register is programmed with LOW, then data from column 0 of the Display Data Memory will be output from SEG0. This type of mapping is called *normal mapping*.

By use of this register, the flexibility of component placement and routing on a PCB can be increased.

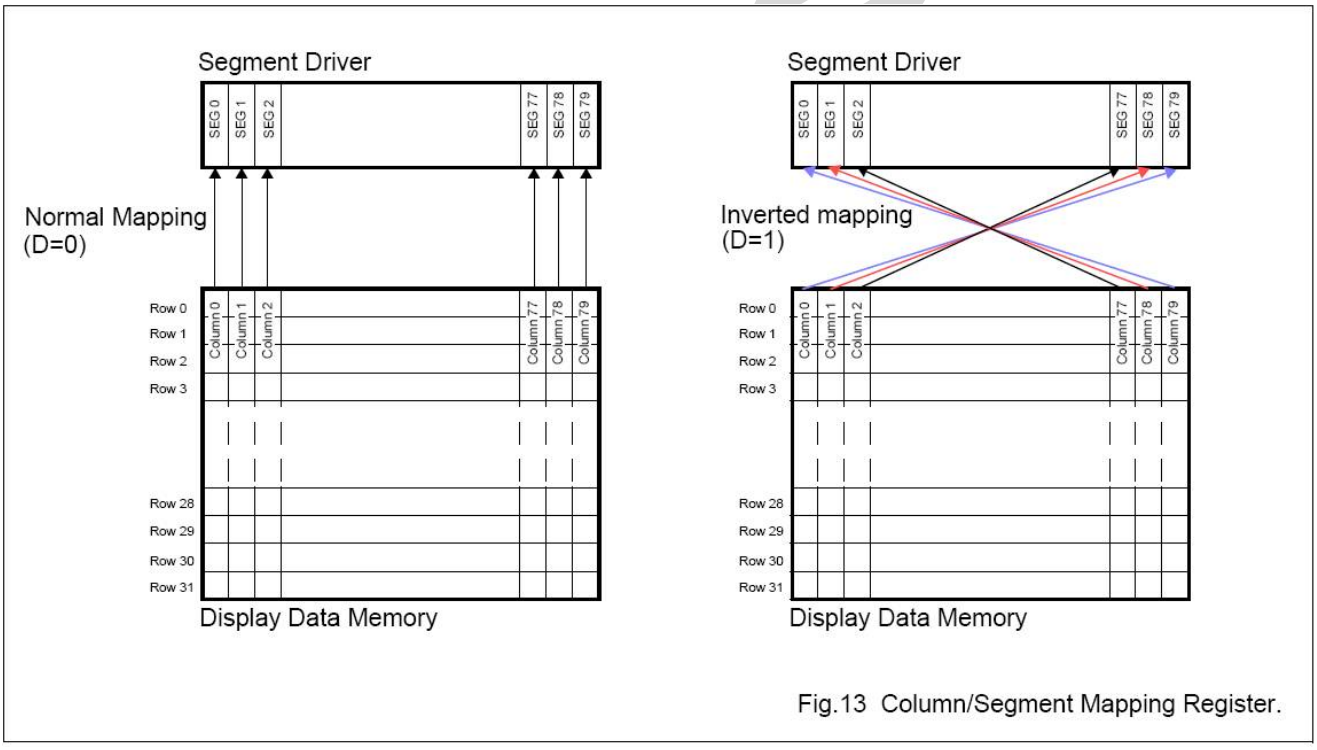


Fig.13 Column/Segment Mapping Register.

To program this register, the setting of the control bus is given in Table 10 and the setting of the data bus is given in Table 11.

Table 10 The setting of the control bus for programming the Column/Segment Mapping Register

C/D	E/(RD)	R/W(WR)
0	1	0

Table 11 The setting of the data bus for programming the Memory/Segment Mapping Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	0	1	0	0	0	0	D

The least significant bit D can be programmed with either 0 or 1. Therefore, the codes are A0 Hex or A1 Hex.

4.4.7 Static Drive ON/OFF and the Static Drive ON/OFF register

The Static Drive ON/OFF Register is a 1-bit register. It is used to turn ON or OFF the *Static Drive Mode* of the SBN1661G_X. When this register is programmed with HIGH, *Static Drive Mode* is turned ON and the device enters into *Static Drive Mode*, in which the internal clock circuitry is disabled and the switching of the internal logic is suspended. When this register is programmed with LOW, *Static Drive Mode* is turned OFF and the chip returns to normal operation.

This register is used in combination with the Display ON/OFF register to make the current consumption of the LCD module reduced to almost static level. By turning OFF the display and turning ON the static drive mode,the chip is configured into the following state:

all COMMON and SEGMENT outputs are set to VDD,

on-chip oscillator or external clock is inhibited and internal logic circuit stays idle,

OSC2 is in floating state (please refer to Section 11 , On-chip RC Oscillator), and

the state of registers and the data of the Display Data Memory are kept unchanged.

In addition to turning ON the static drive mode and turning OFF the display, to really reduce the power consumption of the LCD module, the host microcontroller should also send out a power-save signal to turn off the PNP transistor in the bias circuit, such that the current flow from VDD to VEE can be cut off, as shown in Fig. 14.

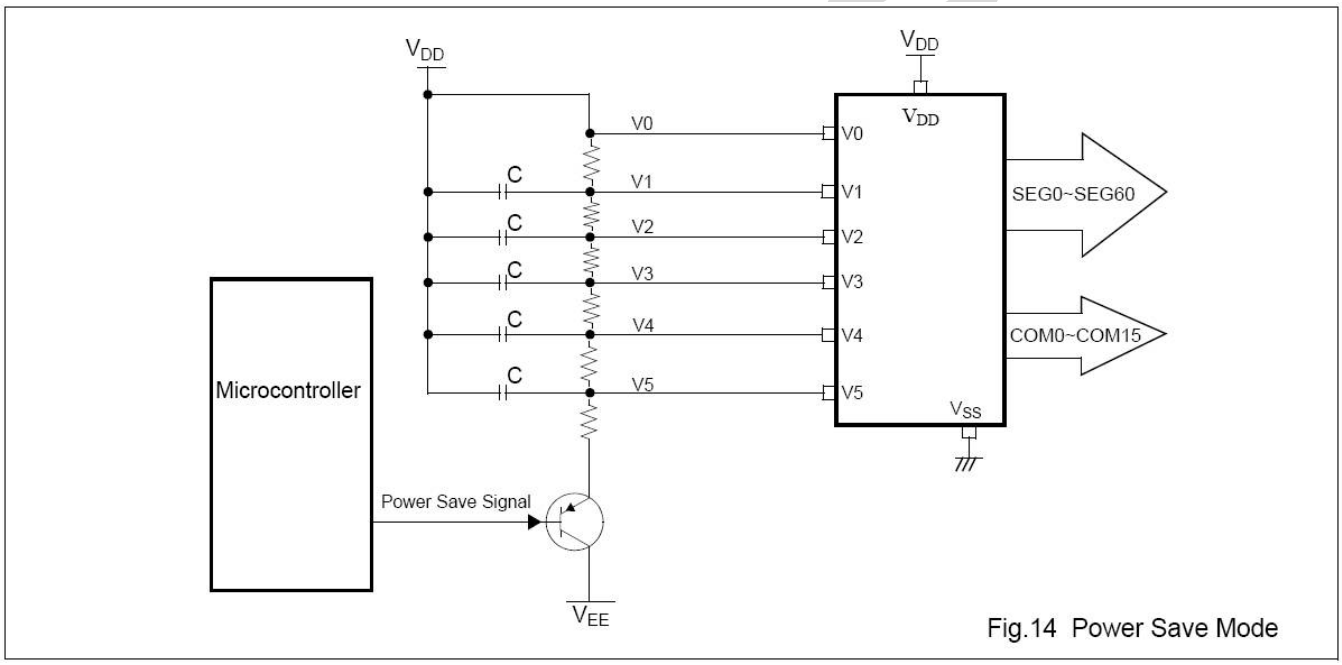


Fig.14 Power Save Mode

To program this register, the setting of the control bus is given in Table 12 and the setting of the data bus is given in Table 13.

Table 12 The setting of the control bus for programming the Static Drive ON/OFF Regist

C/D	E/(RD)	R/W(WR)
0	1	0

Table 13 The setting of the data bus for programming the Static Drive ON/OFF Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	0	1	0	0	1	0	D

The least significant bit D0 can be programmed with either 0 or 1. Therefore, the code is A4 Hex or A5 Hex.

4.4.8 Select Duty and the Select Duty Register

The Select Duty Register is a 1-bit register. If it is programmed with HIGH, 1/32 display duty is selected. If it is programmed with LOW, 1/16 display duty is selected.

To program this register, the setting of the control bus is given in Table 14 and the setting of the data bus is given in Table 15.

Table 14 The setting of the control bus for programming the Select Duty Register

C/D	E/(RD)	R/W(WR)
0	1	0

Table 15 The setting of the data bus for programming the Select Duty Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	0	1	0	1	0	0	D

The least significant bit D can be programmed with either 0 or 1. Therefore, the code is A8 Hex or A9 Hex.

In a Master-Slave connection using the SBN1661G_M18 or the SBN1661G_M02 as the master, COM0~COM15 will be from the master and COM16~COM31 will be from the slave. The Select Duty Register of both the Master and the Slave should be programmed with HIGH to select 1/32 duty. Fig.15 shows the COMMON sequence of this connection.

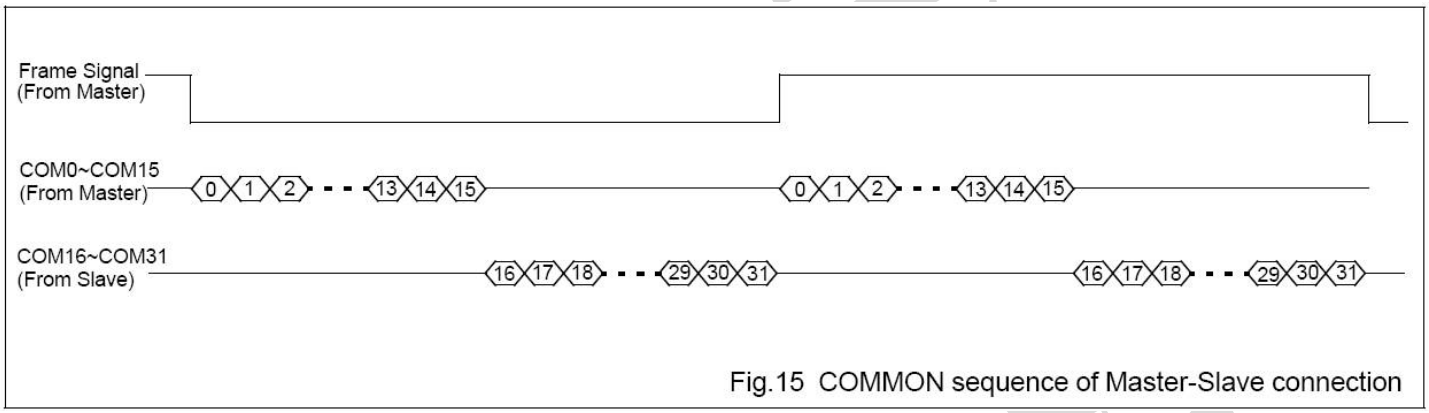


Fig.15 COMMON sequence of Master-Slave connection

This register is not available in the SBN0080G_S18 and the SBN0080G_S02, because both the devices are purely Segment Drivers and their duty cycle is decided by the FR and the CL from the master.

4.4.9 Status Read and Status Register

The Status Register shows the current state of the SBN1661G_X. It can be read by the host microcontroller. Bit 7~4 shows the status and Bit 3~0 are always fixed at 0.

To read the Status Register, the setting of the control bus is given in Table 16, the bit allocation is given in Table 17 and the description for each bit is given in Table 18.

Table 16 The setting of the control bus for reading the Status Register

C/D	E/(RD)	R/W(WR)
0	0	1

Table 17 The Status Register bit allocation

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
BUSY	MAPPING	ON/OFF	RESET	0	0	0	0

Table 18 The Status Register bit description

Bit	Description
BUSY	BUSY=1 indicates that the SBN1661G_X is currently busy and can not accept new command or data. The SBN1661G_X is executing a command or is in the process of reset. BUSY=0 indicates that the SBN1661G_X is not busy and is ready to accept new command or data.
MAPPING	MAPPING=1 indicates that the Column/Segment Mapping Register has been programmed with a value of “1” and the SEG0 is mapped to Column 79 of the Display Data Memory (inverted mapping). MAPPING=0 indicates that the Column/Segment Mapping Register has been programmed with a value of “0” and the SEG0 is mapped to Column 0 of the Display Data Memory (normal mapping).
ON/OFF	The ON/OFF bit indicates the current of status of display. If ON/OFF=0, then the display has been turned ON. If ON/OFF=1, then the display has been turned OFF. Note that the polarity of this bit is inverse to that of the Display ON/OFF Register.
RESET	RESET=1 indicates that the SBN1661G_X is currently in the process of being reset. RESET=0 indicates that the SBN1661G_X is currently in normal operation.

5. NOTES

▪ Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizing plate of the display is very fragile; handle it very carefully

Mounting and Design

- Mount the module by using the specified mounting part and holes.
- To protect the module from external pressure, leave a small gap by placing transparent plates (e.g. acrylic or glass) on the display surface, frame, and polarizing plate
- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

Storage

- Store the module in a dark place where the temperature is 25 °C±10 °C and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

Cleaning

- Do not wipe the polarizing plate with a dry cloth, as it may scratch the surface.
- Wipe the module gently with soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetoe) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.

6. OPERATION PRECAUTIONS

Any changes that need to be made in this specification or any problems arising from it will be dealt with quickly by discussion between both companies.

7. LCM Dimension