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GI FAR TECHNOLOGY CO.,LTD
No. 81, Dongfeng St, Shulin District, 23874, New Taipei City, Taiwan, R.O.C.

SPECIFICATIONS

CUSTOMER : _____

MODEL NO. : GFE122032I-GPNE

VERSION : B

DATE : 2017.03.24

CERTIFICATION : ROHS

CUSTOMER SIGN : _____

QA Approved By	Approved By	Prepared By	Prepared By

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Data(y/m/d)	Ver.	Description	Note	page
2012.07.05	A	Specification released		
2017.03.24	B	修改公司抬頭、格式統一		

CONTENTS

1. SCOPE

This specification covers the engineering requirements for the GFE122032I-GPNE liquid crystal module.

2. PRODUCT SPECIFICATIONS

2.1 General

- 122 × 32 dot matrix LCD
- **STN (GRAY)**, **Positive** mode LCD panel
- **Transflective** Wide temperature type
- 6 o'clock
- Multiplexing driving : 1/32duty, 1/6bias
- Controller IC : **SBN1661G** or Compatible
- Backlight: **NO Backlight**

2.2 Mechanical Characteristics

Item	Value	Unit
Number of dots	122X32	Dot
Dot size	0.4 X0.45	mm
Dot pitch	0.44 X0.49	mm
Module dimension	84(W) X 44(H) X 13.7(T)	mm
Viewing Area	60 (W) X 18 (H)	mm
Active Area	53.64 (W) X 15.64 (H)	mm
Module	NO Connector	

2.3 Absolute Maximum Ratings (Without LED back-light)

Characteristic	Symbol	Unit	Value
Operating Voltage (logic)	V_{DD}	V	-0.3 to +7.0
Input Voltage	V_{IN}	V	-0.3 to V_{DD}+0.3

Note 1: Referenced to V_{SS}=0V

2.4 Electrical Characteristics (Without LED back-light)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage(logic)	V_{DD}-V_{SS}	--	4.7	5.0	5.3	V
Input Voltage	V_{IH}	--	0.8V_{DD}	--	V_{DD}	V
	V_{IL}	--	V_{SS}	--	0.2V_{DD}	
Output Voltage	V_{OH}	I_{OH}=-0.1mA	0.8V_{DD}	--	V_{DD}	V

2.5 Optical Characteristics Absolute maximum ratings

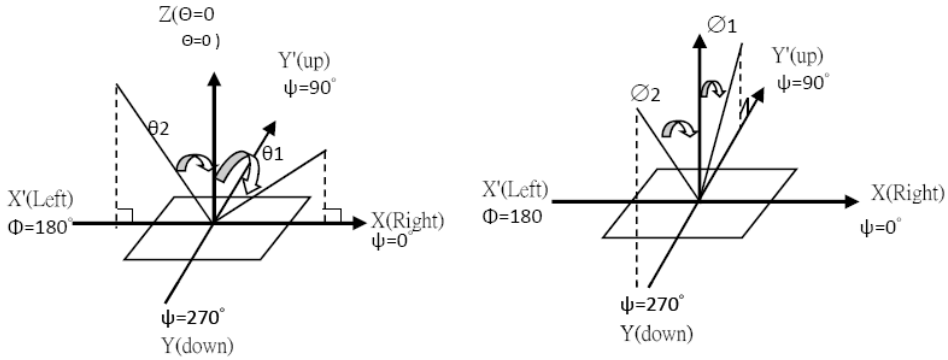
Item	Symbol	Rating	Unit
Operating temperature range	Top	-20~70	°C
Storage temperature range	Tst	-30~80	°C

2.6. Optical Characteristics

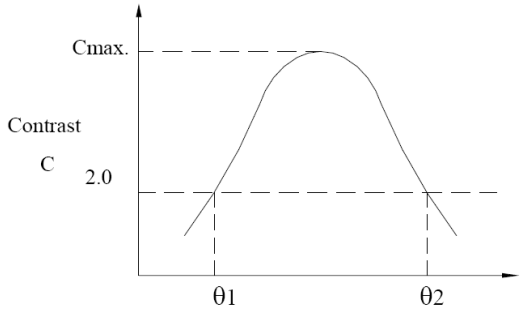
1/32 duty, 1/6 bias, Vop=4.6 V, Ta=25℃

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Driving voltage	Vop		--	4.6	--	
Viewing angle	θ1、θ2	C≥2.0,∅=0° C	30°	-	-	Notes 1 & 2
Contrast	C	θ=5°, ∅=0°	2.0	-	-	Note 3
Response time(rise)	ton	θ=5°, ∅=0°	-	-	260ms	Note 4
Response time(fall)	toff	θ=5°, ∅=0°	-	-	380ms	Note 4

Note 1: Definition of angles θ and ∅

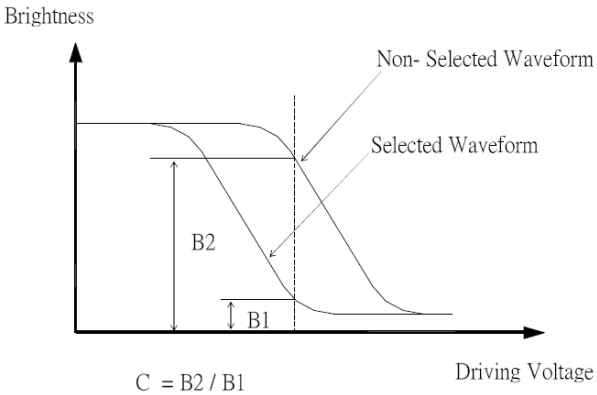


Note 2: Definition of viewing angles θ1 and θ2



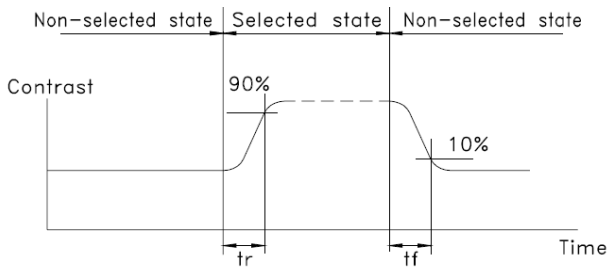
Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the same

Note 3: Definition of contrast C



C = B2 / B1

Note 4: Definition of response time



Note: Measured with a transmissive LCD panel which is displayed 1 cm^2

V_{OPR} : Operating voltage f_{FRM} : Frame frequency
t_{ON} : Response time (rise) t_{OFF} : Response time (fall)

3. RELIABILITY

NO.	ITEM	CONDITION		STANDARD	NOTE
1	High Temp. Storage	80℃	120 hrs	Appearance Without defect	
2	Low Temp. Storage	-30℃	120 hrs	Appearance Without defect	
3	High Temp. & High Humi. Storage	40℃ 90% RH	120 hrs	Appearance Without defect	
4	High Temp. Operating Display	70℃	120 hrs	Appearance Without defect	
5	Low Temp. Operating Display	-20℃	120 hrs	Appearance Without defect	
6	Thermal Shock	-20℃, 30min. → 70℃,30min. (1cycle)		Appearance Without defect	10 cycles

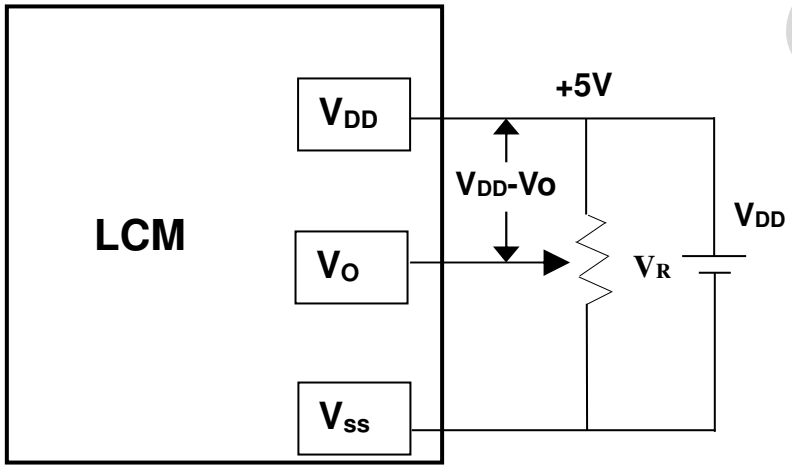
** Dissipation current, contrast and display functions
** Polarizing filter deterioration, other appearance defects
** The function test shall be conducted after 4hours storage at the normal temperature and humidity after remove from the test chamber.

4. OPERATING INSTRUCTIONS

4.1 Input signal Function

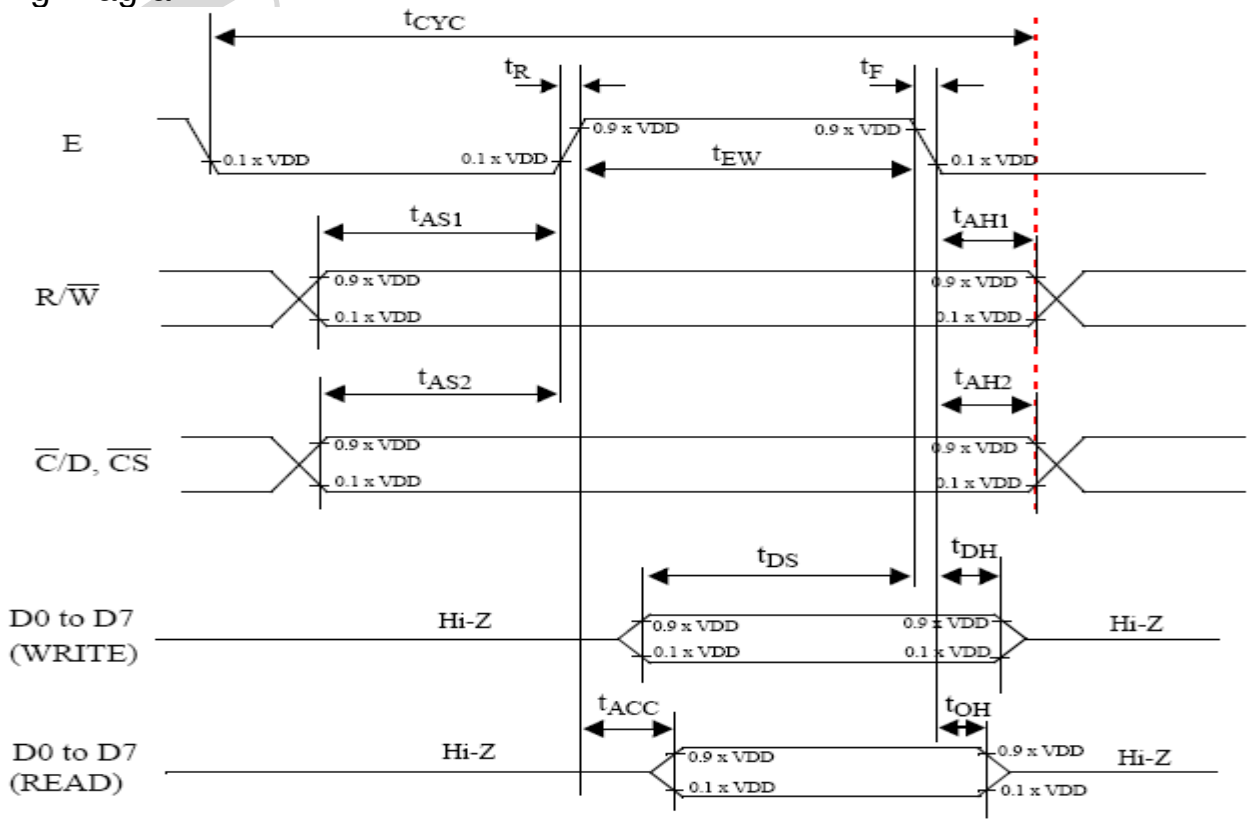
Pin No	Symbol	Function
1	Vss	Signal ground (GND)
2	Vdd	Power supply for logic (+5V)
3	Vo	Operating voltage for LCD (variable)
4	A0	Start enable signal to read or write the data
5	CS1	Chip1 enable (segment 1 to segment 64),Active high
6	CS2	Chip2 enable (segment 65 to segment 128),Active high
7	NC	NC
8	NC	NC
9	R/W	Data read & write
10-13	DB0~DB3	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCD module.
14-17	DB4~DB7	Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCD module. DB7 can be used as a busy flag.
18	RST	Reset signal
19	NC	NC
20	NC	NC

4.2 Voltage Generator Circuit



V_{DD}-Vo : LCD Driving Voltage
V_R : 10K~20K

4.3 Timing Diagram



symbol	parameter	min.	max.	test conditons	unit
t_{AS1}	Address set-up time with respect to R/$\overline{W}$	20			ns
t_{AS2}	Address set-up time with respect to $\overline{C}$/D, $\overline{CS}$	20			ns
t_{AH1}	Address hold time with respect to R/$\overline{W}$	10			ns
t_{AH2}	Address hold time respect with to $\overline{C}$/D, $\overline{CS}$	10			ns
t_F, t_R	Enable (E) pulse falling/rising time		15		ns
t_{CYC}	System cycle time	1000		Note 1	ns
t_{EWR}	Enable pulse width for READ	100			ns
t_{EWW}	Enable pulse width for WRITE	80			ns
t_{DS}	Data setup time	80			ns
t_{DH}	Data hold time	10			ns
t_{ACC}	Data access time		90	CL= 100 pF.	ns
t_{OH}	Data output hold time	10	60	Refer to Fig. 23.	ns

4.4.DISPLAY CONTROL INSTRUCTIONS AND REGISTERS

4.4.1 Registers and their states after hardware RESET

The SBN1661G_X has a set of registers. To ensure proper operation of the devices, these registers must be programmed with proper values after hardware reset.

The registers and their states after RESET is given in Table 1.

Table 1 Registers and their states after RESET

Register Name	Description	States after RESET
Display ON/OFF Register	The Display ON/OFF Register is a 1-bit register. After RESET, its value is LOW and, therefore, the LCD display is turned OFF.	0
Display Start Line Register	The Display Start Line Register is a 6-bit register. After RESET, its value is 0 0000 and Row0 of the Display Data Memory is mapped to COM0.	00 0000
Page Addres Register	The Page Address Register is a 3-bit register. After RESET, its value is 11 and, therefore, it points to Page 7 of the Display Data Memory.	111
Column Address Register	The Column Address Register is a 7-bit register. After RESET, its value is 000 0000 and, therefore, it points to column 0 of the Display Data Memory.	000 0000
Static Drive ON/OFF Register	The Static Drive ON/OFF Register is a 1-bit register. After RESET, its value is LOW and static display is turned OFF.	0
Duty Select Register	The Duty Select Register is a 1-bit register. After RESET, its value is HIGH and 1/32 display duty is selected.	1
Column/Segment Mapping Register	The Column/Segment Mapping Register is a 1-bit register. After RESET, its value is LOW and normal mapping is selected.	0
Status Register	The Status Register shows the current state of the SBN1661G_X. It is a 4-bit register, with each bit showing the status of a programmed function.	0000 0000

4.4.2 Display ON/OFF and the Display ON/OFF Register

The Display ON/OFF Register is a 1-bit Register. When this bit is progammed to HIGH, the display is turned ON. When this bit is programmed to LOW, the display is turned OFF and all COMMON and SEGMENT outputs are set to VDD.

To program this register, the setting of control bus is given in Table 2 and the setting of the data bus is given in Table 3.

Table 2 Setting of the control bus for programming the Display ON/OFF Register

C/D	E/(RD)	R/W(WR)
0	1	0

Table 3 Setting of the data bus for programming the Display ON/OFF Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	0	1	0	1	1	1	D0

When D0=1, the code is AF(Hex) and the display is turned ON. When D0=0, the code is AE(Hex) and the display is turned OFF.

4.4.3 Display Start Line and the Display Start Line Register

The Display Start Line Register is a 5-bit Register. It points at the first row of a block of the Display Data Memory, which will be mapped to COM0. The length of the block of the memory can be 32 rows or 16 rows, which is decided by the Duty Select Register. For example, if the Display Start Line Register is programmed with 00010 (decimal 2) and display duty is 1/32, then Row2 of the Display Data Memory will be mapped to COM0 of LCD panel, Row3 to COM1, Row4 to COM2, Row30 to COM28, Row31 to COM29, Row0 to COM30, and finally Row1 to COM31, as illustrated in Fig. 11. However, in this case, only Row2~Row17 can be displayed on COM0~COM15, as COM16~COM31 are not availabe from the chip.

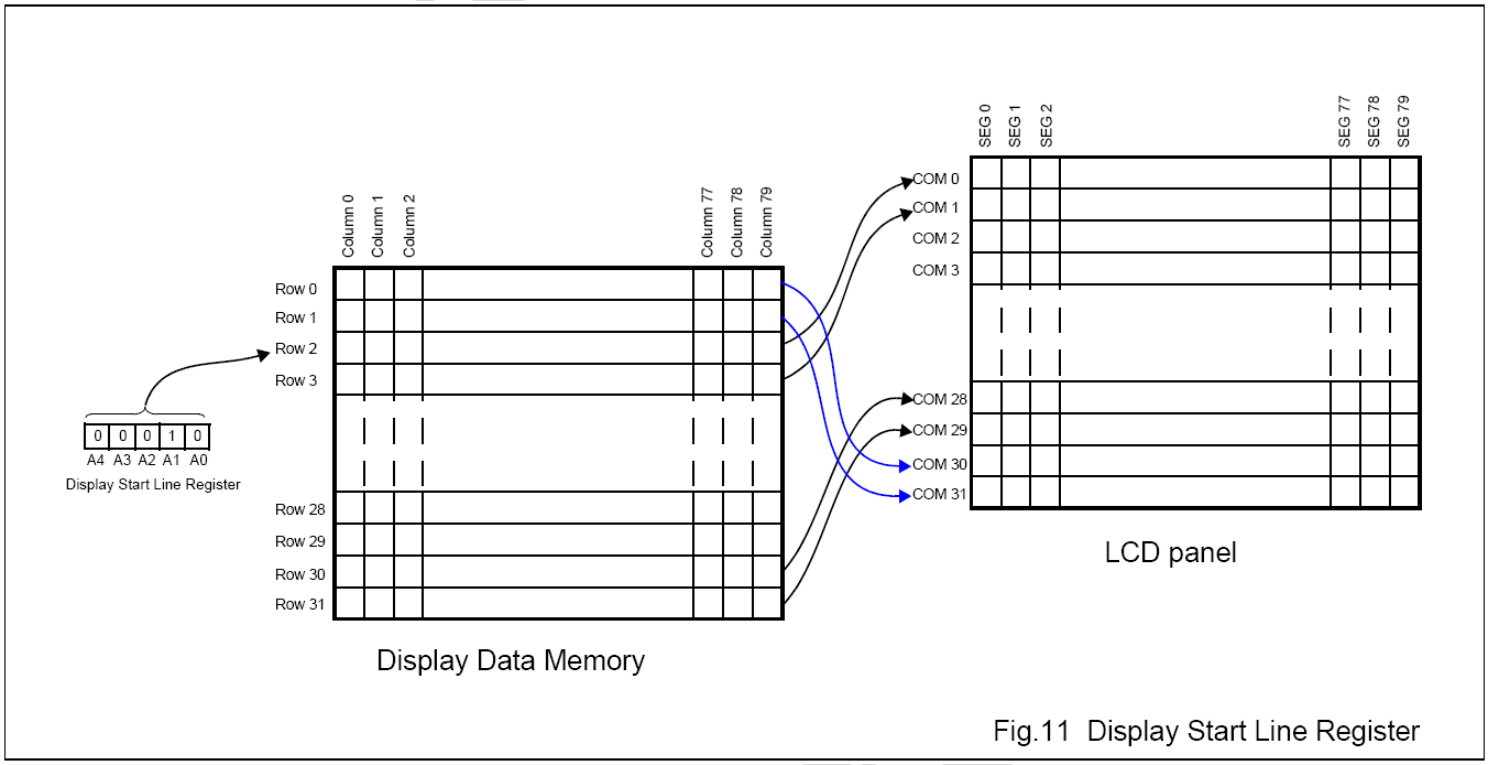


Fig.11 Display Start Line Register

To program this register, the setting of the control bus is given in Table 4 and the setting of the data bus is given in Table 5.

Table 4 The setting of the control bus for programming the Display Start Line Register

C/D	E/(RD)	R/W(WR)
0	1	0

Table 5 The setting of the data bus for programming the Display Start Line Register

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	1	0	A4	A3	A2	A1	A0

A4, A3, A2, A1, and A0 are Start Line address bits and they can be programmed with a value in the range from 0 to 31. Therefore, the code can be from 1100 0000 (C0 Hex) to 1101 1111 (DF Hex).